Integrated Printed Circuit Board Planar Magnetics DC/DC Converters

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General Description

The demo board for the Si9114A high-frequency switchmode controller demonstrates the circuit's high voltage and high switching frequency characteristics. The circuit is designed to operate over an input voltage range of 30- to 72-V, DC, at 750-kHz. The high input voltage range is ideal in communications applications circuits where a −48 V DC "battery" voltage and an ac ring voltage may appear at the input. The high-frequency switching capability enables the use of low-value inductors, such as the planar magnetics featured on this demo board.

The circuit was design to provide a 5 V±5% regulated output voltage at a maximum load of 4 A. Also featured on the demo board are TEMIC's LL4148 small-signal diode and the TCMT1020 opto-coupler. Circuit performance is easily evaluated using the edge connectors for input and output and the 11 clearly marked test points.

Two important cautions:

- Be careful to limit the maximum input voltage to 72 V and the maximum output load to 4 A. The load resistor or resistors, if used, must not be less than 1.25 Ω and must be capable of handling 20 W.
- Do not power up the board without a load across the output.

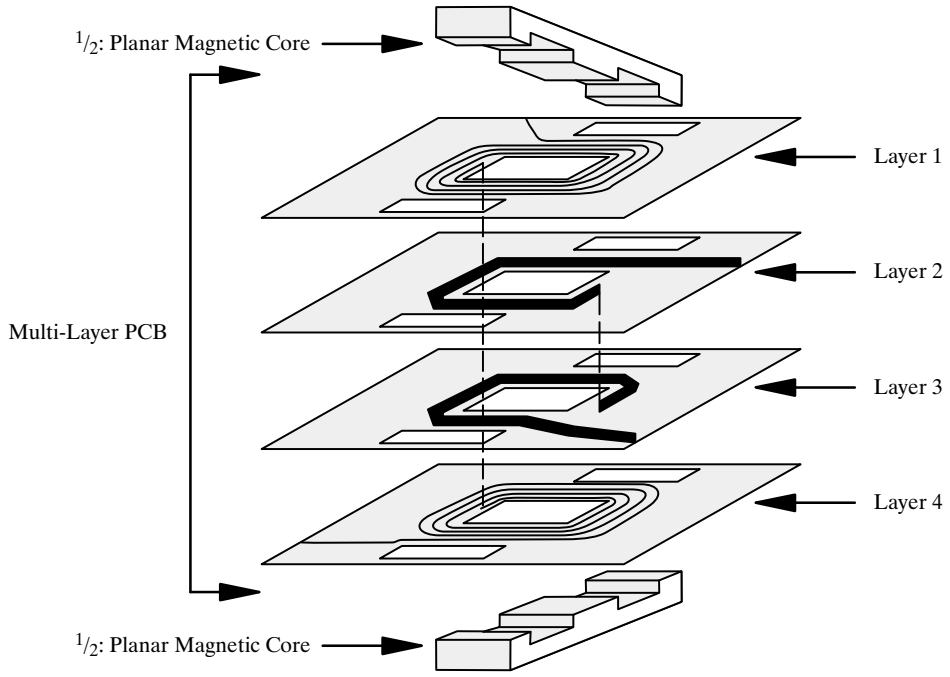


Figure 1. Integrated PCB Planar Transformer

Using Planar Magnetics

Planar magnetics have been gradually introduced into high-frequency converters over the last few years due to their high performance and small size. Previously it was assumed that planar magnetics were only suitable for high-frequency *quasi*-resonant topologies. But the advent of low power consumption, high-performance current mode PWM controllers, such as the Si9114AA, has allowed this family of magnetic device to be extended to the more popular forward and flyback converters.

Switching Frequency Selection

Planar magnetics require operation at high frequency to maintain a low inductance value. At the same time, they are impractical at more than 6 to 8 turns in a single layer. The secret to a good planar design is using a switching frequency that is low enough to reduce losses, but high enough to minimize the number of turns. Optimal designs will operate between 250 kHz and 1 MHz and above.

Design Example: 15-W Forward Converter Design at 750 kHz

To evaluate this technology, a 15-W converter was built using a six-layer circuit board. Utilizing a resonant reset technique, the circuit avoids the use of a reset winding and produces benign soft reset waveforms during the reset period.

An opto-coupler was used in conjunction with a TL431 to achieve voltage isolation between input and output.

The target specification was:

V_{IN} = 36-to-72 V dc	Input Voltage Minimum/Maximum
V_{OUT} = 5-V dc	Output Voltage
F_{sw} = 750 kHz	Switching Frequency
I_{OUT} = 0 to 3A	Output Current Minimum/Maximum
DV_{OUT} = < 50 mV	Ripple Voltage
η (%) = >80%	Target Efficiency

The transformer design can now be undertaken as follows:

First determine the exact voltage that will be applied to the primary, and that required from the secondary to meet the performance requirements. The minimum primary voltage can be determined by subtracting all the losses in the primary from the input voltage.

The input power, assuming 80% efficiency, will be:

$$P_{IN} = \frac{P_{OU}}{\eta} = \frac{15\ W}{0.8} = 18.75\ W \quad [1]$$

At low line input, with 36 V, the input current will be:

$$I_{DCIN} = \frac{P_{IN}}{V_{INMIN}} = \frac{18.75\ W}{36} = 0.52\ A \quad [2]$$

The average input current switched in the primary will then be:

$$I_{AV} = \frac{I_{DC}}{\delta_{MAX}} = \frac{0.52\ A}{0.48} = 1.08\ A \approx 1.1\ A \quad [3]$$

With the Siliconix Si9420DY MOSFET, maximum on-resistance is 1 Ω. During conduction, the voltage developed across this device will thus be 1.1 × 1 = 1.1 V. The series sense resistor for the current mode comparator will also develop approximately 1.25 V when close to the trip threshold, and hence must also be added to the losses.

The total primary voltage available to the transformer is therefore:

$$V_{PRIM} = V_{INMIN} - V_{MOSFET} - V_{SENSE} = 36\ V - 1.1\ V - 1.25\ V = 33.65\ V \quad [4]$$

Now calculate the voltage required from the secondary to achieve the correct output voltage at full load and low line.

The output is defined as 5 V, but some margin of adjustment might be desirable. For example, a ±2.5% margin would require and output of V_{OUT} = 5.125 V.

The output choke DC resistance has been calculated (see later in test results) as 25 mΩ. With 4 A of current, this would mean a voltage drop V_{CHOKE} of 100 mV.

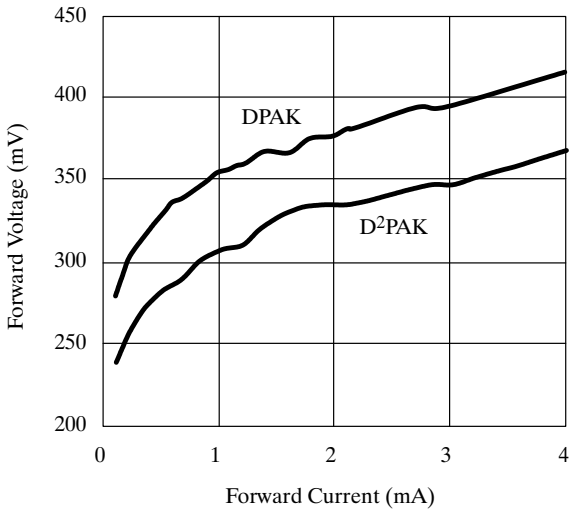


Figure 2. Forward Voltage Drop of Schottky Diodes

The Schottky diodes—typically contributing the largest share of losses in the converter—will have a forward voltage drop between 0.35 and 0.6 V, depending on the manufacturer and on the actual current at temperature. In examples tested, recent D²PAK and DPAK devices were compared. The DPAK 5-A, 40-V device (D5SC4M[1]) had a forward voltage drop of less than 0.45 V at 4 A, and was thus selected. To avoid any thermal effects, this voltage was measured by pulsing the diodes, and was taken at room temperature. In practice, under load and due to self heating, voltage drop will be lower, due to the temperature coefficient of the diode.

The voltage required at the secondary of the transformer can now be determined by adding all the losses in series from the secondary of the transformer to the output voltage and using the maximum duty cycle δ_{MAX} that will be used:

$$V_{SEC} = \frac{V_{OUT} + V_{CHOKE} + V_{DIODE}}{\delta_{MAX}}$$

$$V_{SEC} = \frac{5.125 + 0.1 + 0.45}{0.48} \quad [5]$$

$$V_{SEC} = 11.823\ V \approx 11.8\ V$$

The duty cycle was set to 0.48 in order to allow for switching transition times, and minimum on time.

This is the peak secondary voltage required to obtain the correct output voltage.

Now that both the primary and the secondary of the transformer voltages are known, the turns ratio will be:

$$N = \frac{V_{PRIM}}{V_{SEC}} = \frac{33.65}{11.8} = 2.85 \quad [6]$$

The transformer design can now be completed as follows:

First select a suitable core size. In this case, the PL20 has the following characteristics:

Effective Area: $0.4\ cm^2$

Effective Volume: $0.88\ cm^3$

Overall dimensions: $10 \times 18 \times 6$ mm

Material : Philips 3F4

Calculate the turns ratio using Faraday's equation, assuming :

B_{MAX} = 70 mT (Emperical first choice)

V_{INMIN} = 36 V

T_{ONMAX} = 640 ns (Fs = 750 kHz and Dmax = 0.48)

$$N_{MIN} = \frac{V_{INMIN} \times T_{ONMAX}}{B_{MAX} \times A_{EFF}}$$

$$N_{MIN} = \frac{36\ V \times 640\ ns}{70\ mT \times 0.4\ cm^2} \quad [7]$$

$$N_{MIN} = 8.22\ Turns$$

This is the minimum number of turns that should be used for the selected operating flux density. In practice, either eight or nine turns will have to be selected, with higher or lower operating flux density.

The core loss for these operating conditions can be determined from:

$$P_V = 12 \times 10^{-2} \times F_{SW}^{1.75} \times B_{MAX}^{29} \times K$$

where [8]

$$K = \left(0.95 \times 10^{-4} \times T^2\right) - \left(1.1 \times 10^{-2} \times T\right) + 1.15$$

and T is the operating ambient temperature[2].

[1] Samples courtesy of Schindengen UK.
[2] Data supplied coutesy of Philips Components.

For T = 60C, K = 0.832. With F_{sw} = 750 kHz and B_{MAX} = 70 mT this yields:

$$P_V = 0.854 \times 10^{-3} \text{ W/m}^3 \text{ or } 0.854 \text{ W/m}^3 \quad [9]$$

This loss is the loss associated with a *peak-to-peak* flux swing of 70 mT. In this case, as the core is driven in one quadrant only, the actual core loss is half of the value calculated.

As this core is 0.88 cm^3 then the core loss will be :

$$\frac{(0.88 \times 0.854)}{2} = 0.375 \text{ W} \quad [10]$$

which represents approximately 10% of the total converter losses. If the core and copper losses were identical, then the total losses would represent 20% of all the losses, which is acceptable as a first starting point.

It must be pointed out that in calculating these parameters, the use of a spreadsheet is recommended, as the design is entirely empirical and iterative in nature, and repeated calculations are very common in order to arrive at the right selection of core and number of turns. The spreadsheet allows repeated calculations to be displayed simultaneously, thus allowing a judgment on which design is the best.

Now that the minimum turns have been calculated, and the turns ratio has been determined, the secondary turns can be obtained as follows:

$$N_{SEC} = \frac{N_{PRIM}}{\text{Turns Ratio}} = \frac{9}{2.85} = 3.15 \quad [11]$$

It now becomes apparent that planar magnetics, like all other higher-frequency low-turns count transformers, have a significant disadvantage due to the large voltage per turn count. Indeed, most designs will require a compromise among turns count, losses, and practicality.

In this case, as the number above is the minimum turns required to obtain the correct output voltage, it becomes apparent that it will be necessary to use eight turns on the primary in order to satisfy the turns ratio requirement. The new number of secondary turns will thus be:

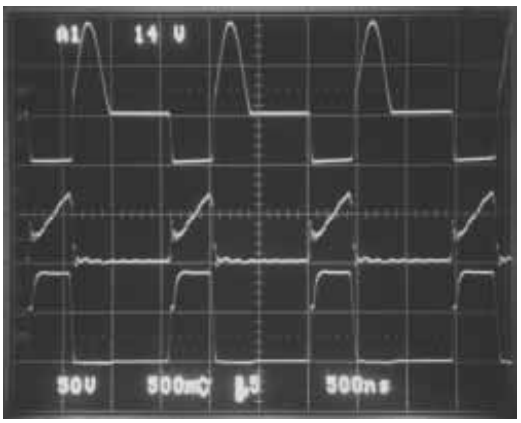
$$N_{SEC} = \frac{N_{PRIM}}{\text{Turns Ratio}} = \frac{8}{2.85} = 2.8 \quad [12]$$

Now the next highest whole number turns can be used, i.e. three.

To supply the Si9114A, the bias winding will also require three turns, as we have already determined that three turns will generate a voltage near 11.8 V peak, which will reduce to 11 V if used in a peak charging circuit.

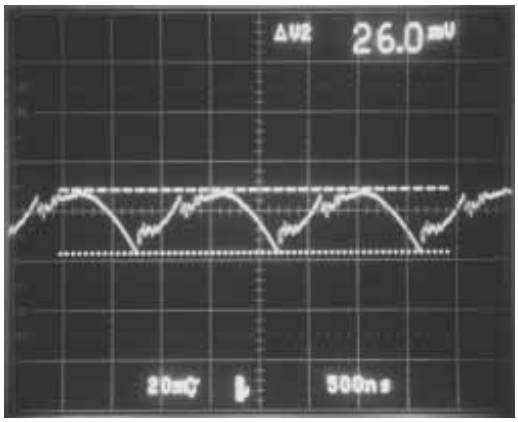
The primary switching waveforms are extremely clean on turn-off, and core saturation is prevented by using the resonant reset technique. These switching waveforms are shown in Figure 3.

The output ripple was measured using a noise probe with very short wires (See Figure 4):



Top: V_{DS} @ 50 V/div
Middle V_{SENSE} @ 500 mV/Div
Bottom: V_{GS} @ 5 V/div
Time: 500 ns/div

Figure 3. Voltage Waveforms of Planar Converter



Trace: 20 mV/Div, 500 ns/Div

Figure 4. Output Ripple of Converter Under Load

The converter was subjected to a short circuit, and the frequency of the converter was measured with normal load and short circuit load. Figure 5 shows a double exposure of the same waveform for normal and shorted operation. Under normal operation the frequency is 700 kHz, and under short circuit, the frequency changes to 160 kHz.

The transient response of the circuit under switched load was tested and found to be excellent. With just 15 µF, very acceptable transient response times are possible due to the high unity gain bandwidth of the complete circuit. In practice, even better response can be obtained without the use of opto-couplers, as these devices introduce phase shifts at higher bandwidths. The response time for a step load from 1 to 2.5 A was measured at 35 µs (See Figure 6).

The efficiency of the converter under load and line variations was measured, and found to be as follows:

The following measurements were taken from the PCB:

Planar Transformer

Primary Inductance	=	110 µH
Primary DC resistance	=	174 mΩ
Secondary Inductance	=	6.86 µH
Secondary Resistance	=	10.2 mΩ

Planar Choke

DC Resistance	=	17.5 mΩ
Inductance	=	4.5 µH

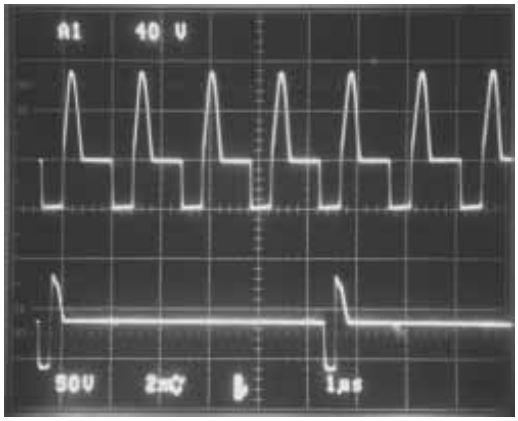


Figure 5. Frequency Shift Under Short Circuit

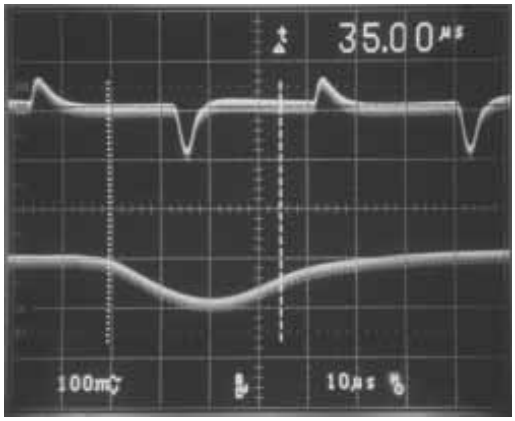


Figure 6. Step Response

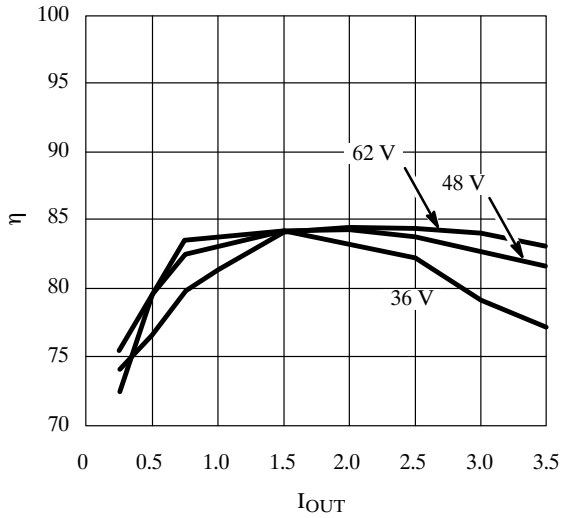


Figure 7. Efficiency Under Full Load with Different Input Voltages

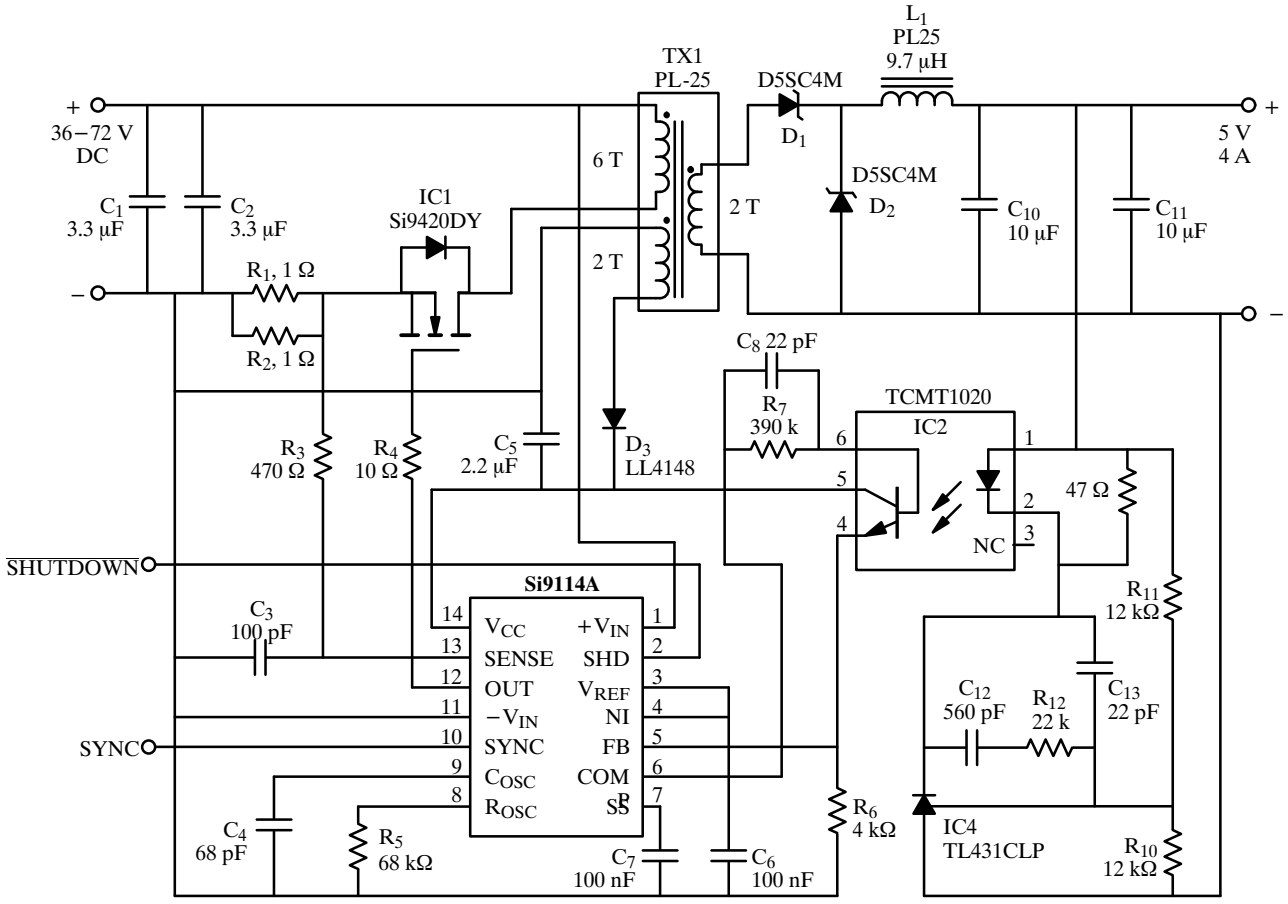


Figure 8. Complete Schematic Diagram

References

1. Mohandes, Bijan. 1993. Designing high-frequency dc-to-dc converters with the Si9114A. Siliconix Application Note AN701.

2. Blattner, Robert. 1992. High efficiency buck converter for notebook computers. Siliconix Application Note AN___.

3. McLymann, Colonel Wm. Designing magnetic components for high frequency dc-dc converters. Kg Magnetics, ISBN #1-883107-00-8

4. Murakami, Naoki and Yamasaki, Mikio, 1988. Analysis of a resonant reset condition for a single ended forward converter. PESC88 Record (April) CH 2523-9/88/0000-1010 $1.00 © 1988 IEEE.

5. Advance Ferrite Technical Data sheet.Advance Ferrite Ltd.,Unit 13 Rumer Hill Ind.Est, Cannock, Staffs, Tel +44-1543-466700, Fax +44-1543-462-9380

6. Carsten, Bruce [Oltronics Canada Ltd, 6-5707 Sideley St., Burnaby, BC,Canada, V5J 5E6], 1990. Design techniques for transformer active reset circuits at high frequencies and power levels. High-Frequency Power Conference Proceedings, May.